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TITLE: High-speed processor system having bus arbitration mechanism

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

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COUNTRY	APPL-NO	APPL-DATE
JP	9-049758	February 17, 1997
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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4698753	October 1987	Hubbins et al.	709/209
☐	5280587	January 1994	Shimodaira et al.	713/600
☐	5668956	September 1997	Okazawa et al.	710/126

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☐	5729703	March 1998	Onn et al.	710/126
☐	5764895	June 1998	Chung	709/250
☐	5809259	September 1998	Mitsuishi	710/126

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

A high-speed processor system having a bus arbitration mechanism constructed on a single semiconductor chip. The processor system comprises at least one bus master, a plurality of buses and a plurality of bus slaves. Each bus comprises an independent address bus, an independent data bus and individual data transfer capability. Every bus master comprises a plurality of independent bus interfaces each connected to one of the buses. Each bus slave is connected to a bus that has corresponding data transfer capability. For a system having more than two bus masters, the system further comprises a plurality of bus arbitrators for arbitrating the access of each bus independently. The bus arbitrator receives a bus request signal from each bus master that requests the bus access and issues a bus grant signal to the bus master allowed to access the bus. The bus arbitrator comprises a plurality of priority order information storage devices for storing priority order information for all the bus masters connected to the bus. At every bus cycle, one set of priority order information is selected continuously and cyclically. When more than one bus master requests the bus access at the same time, the bus arbitrator determines which bus master may access the bus according to selected priority order information.

21 Claims, 22 Drawing figures